REMARKS

Claims 1-3, 6-10, 13-21, 25-29, 33, 36-44, and 93-106 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joannopoulos, US 5,955,749, in view of Scherer et al., US 6,711,200, hereinafter "Scherer." Applicants respectfully traverse the rejection.

The Examiner cites Scherer as teaching "a gold and chromium electrode (26, 28) on a semiconductor layer and . . . several methods for creating electrodes on the photonic crystal including specifically a portion of the second electrode (68) is disposed in a region of the second semiconductor layer (62) in which a portion of the plurality of holes are formed."

Claim 1 as amended recites "when forward biased, light is emitted from at least a portion of the active layer disposed beneath a portion of the second electrode." This amendment is supported by, for example, paragraph [0066].

In contrast to claim 1, Scherer specifically teaches that current is injected in the device by an electrode near a defect, but light is emitted from the device in a photonic crystal region AWAY from the electrode, not in the same region as the electrode. For example, column 2, line 6 of Scherer recites:

> A defect is formed in the two-dimensional photonic lattice by removing an air hole and/or adjusting the diameters of the few neighboring air holes. A mode or set of modes depending on the defect geometry, which is highly localized to the defect region, is formed. Photons can escape from the defect cavity by tunneling through the two dimensional photonic crystal, or by leaking out vertically from the waveguide.

The above passage teaches that light is not emitted in the part of the active region underneath the electrode. In contrast, claim 1 recites light is emitted from at least a portion of the active layer disposed beneath a portion of the second electrode. Accordingly, even in combination, Joannopoulos and Scherer fail to teach every element of claim 1.

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Claim 25 is similarly amended and is thus allowable over Joannopoulos and Scherer for at least the same reason as claim 1.

Claims 2, 3, 6-10, 13-21, 93-95, and 99-102 depend from claim 1 and are therefore allowable over Joannopoulos and Scherer for at least the same reasons as claim 1. Claims 26-29, 36-44, 96-98, and 103-106 depend from claim 25 and are therefore allowable over Joannopoulos and Scherer for at least the same reason as claim 1.

In addition, regarding claims 3 and 29, on page 6 of the office action, the Examiner states "Scherer teaches, from figs. 1D and 21B, the light emitting diode wherein said first semiconductor layer (17, 19, or 21) overlies said first electrode layer 64." Since Scherer states at column 13 line 32-33 that layer 64 is an "epitaxially grown . . . n-doped contact layer[]," not an "electrode layer" as recited in claims 3 and 29, the combination of Scherer and Joannopoulos fails to teach this additional element of these claims, thus these claims are allowable over the combination for this additional reason.

Regarding claims 6 and 27, which recite "a surface in one of the plurality of holes has a surface recombination velocity less than 10^5 cm/sec," the Examiner states at page 6 Joannopoulos with Scherer inherently (for a gallium nitride based LED) teaches the light emitting diode wherein said first semiconductor layer, said active layer, and said second semiconductor layer have a surface recombination velocity less than 10^5 cm/sec." Applicants have at least twice supplied evidence that the surface recombination velocity is NOT inherent in the structure, and can be influenced by the manner in which the holes are formed. For example, some fabrication techniques can damage the crystal layer or layers in which the holes are formed, which may increase the surface recombination velocity in a device. Boroditsky et al., *Surface recombination measurements on III-V candidate materials for nanostructure light-emitting diodes*, 87 Journal of Applied Physics, Volume 87, Number 7, pp. 3497-3504, 3500 (2000), cited in previous information disclosure statements, state:

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> In our experiment, the PL of an 'as-grown' GaN sample was first measured to determine the internal quantum efficiency and the surface recombination velocity (SRV), which was found to be S = 2.8 X 10^4 cm/s. The same was then etched in a chemically assisted ion beam etching machine for 1 min in $Ar^+ + Cl_2$, which removed 30 nm from the top cap layer. Figure 3 shows that after etching, . . . SRV increased to S = 7 X 10^4 cm/s.

The above-quoted passage clearly demonstrates that the surface recombination velocity is not inherent to a device, since the same material may have two different surface recombination velocities, depending on how the material was etched.

Though Boroditsky et al. teach surface recombination velocities less than 10^5 cm/sec, Boroditsky et al. is only etching the surface of a c-plane layer of III-nitride crystal. In contrast, forming a plurality of holes necessarily exposes crystal surfaces other than the c-plane. Accordingly, a person of skill in the art would expect that the SRV values given in Boroditsky et al. would have no bearing on the surface recombination velocity of a surface in one of the plurality of holes as recited in claims 6 and 27.

Since a surface recombination velocity less than 10^5 cm/sec is not inherent in the structures taught by Joannopoulos and Scherer, claims 6 and 27 are allowable over these references for this additional reason.

Claims 4 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joannopoulos and Scherer in view of Yoo, US 6,949,395. The Examiner cites Yoo only as teaching "a light emitting diode wherein said first electrode layer (250) partially overlies said first semiconductor layer (140); and said first semiconductor layer (140) overlies a substrate (100A) with a reflective surface (200)." See office action, page 11. As such, the Examiner's analysis of Yoo adds nothing to the deficiencies of Joannopoulos and Scherer with respect to claims 1 and 25, from which claims 4 and 30 depend. Claims 4 and 30 are therefore allowable over the combination of Joannopoulos, Scherer, and Yoo for at least the same reasons claims 1 and 25 are allowable over Joannopoulos and Scherer.

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Claims 5, 22, 23, 31, 45, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joannopoulos and Scherer in view of Tanabe, US 6,735,230. The Examiner cites Tanabe only as teaching "a light emitting diode wherein said first electrode layer (9) partially overlies said first semiconductor layer (3); said second electrode layer (10) is substantially reflective (made from Ni/Al); and said first semiconductor layer overlies a substantially transparent substrate (1)" and "the first semiconductor layer (4) and said second semiconductor layer (6) each comprise at least one layer of a III-nitride material; said active layer (5) comprises InGaN (column 12, lines 54-58); and said first (9) and second (10) electrode layers comprise at least one of Ag, Al, and Au." See office action pages 12 and 13. As such, the Examiner's analysis of Tanabe adds nothing to the deficiencies of Joannopoulos and Scherer with respect to claims 1 and 25, from which claims 5, 22, 23, 31, 45, and 46 depend. Claims 5, 22, 23, 31, 45, and 46 are therefore allowable over the combination of Joannopoulos, Scherer, and Tanabe for at least the same reasons claims 1 and 25 are allowable over Joannopoulos and Scherer.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joannopoulos and Scherer in view of Roberts, US 6,335,548. The Examiner cites Roberts only to teach "a light emitting diode (202) . . . disposed in a package." See office action, page 14. As such, the Examiner's analysis of Roberts adds nothing to the deficiencies of Joannopoulos and Scherer with respect to claim 1, from which claim 24 depends. Claim 24 is therefore allowable over the combination of Joannopoulos, Scherer, and Roberts for at least the same reasons claim 1 is allowable over Joannopoulos and Scherer.

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Should the Examiner have any questions, he is invited to call the undersigned at (408) 382-0480.

Respectfully submitted,

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